Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A computer system, comprising: ~~said computer system having~~
a central processing unit,
~~a~~ core logic connected to said central processing unit,
system random access memory connected to said core logic, ~~and~~
a first AGP bus connected to said core logic, and ~~said apparatus further comprising:~~
an AGP to AGP bridge connecting ~~, said AGP to AGP bridge constructed and arranged to connect~~ at least two AGP-compatible devices to said computer system via said first AGP bus.

2. (Currently amended) A computer system as in claim 1, wherein said first AGP bus ~~is~~ comprises a 32-bit bus or a 64 bit bus.

3. (Canceled).

4. (Currently amended) A computer system as in claim ~~3~~ 2, wherein said AGP to AGP bridge has a PCI interface.

5. (Canceled).

6. (Currently amended) A computer system as in claim 1, wherein said first AGP bus ~~is a~~ comprises the 64-bit bus acting as a first 32-bit AGP bus and a second 32-bit AGP bus, said first and said second 32-bit AGP buses capable of operating concurrently.

7. (Currently amended) A computer system as in claim 1, wherein said first AGP bus ~~is a~~ comprises the 64-bit bus and said AGP to AGP bridge ~~is~~ comprises an ASIC that interfaces directly with said core logic, said first AGP bus ~~behaves~~ behaving as a superset of ~~the~~ a standard 32-bit AGP bus.

8. (Canceled).

9. (Currently amended) A computer system, comprising: ~~said computer system having~~

a central processing unit,
a core logic connected to said central processing unit,
system random access memory connected to said core logic, ~~and~~
a first AGP bus connected to said core logic, and ~~said apparatus further comprising:~~
an AGP to AGP bridge couple to said core logic, said AGP to AGP bridge comprising:
~~a first AGP bus connected to said core logic, said first AGP bus consisting of a 64-bit~~
a bus that is configured as two ~~32-bit~~ lower bit number buses, each of said ~~32-bit~~ lower bit number buses acts as a standard AGP bus to said core logic, each of said ~~32-bit~~ lower bit number bus can operate concurrently with the other of said ~~32-bit~~ lower bit number bus.

10. (Original) A computer system as in claim 9, wherein said AGP to AGP bridge has a PCI interface.

11.-46. (Canceled).

47. (New) A computer system, comprising:

a central processing unit;

a core logic connected to said central processing unit;
a system random access memory connected to said core logic; and
a first AGP bus connected to said core logic; and
means for bridging at least two AGP-compatible devices to said computer system via said first AGP bus.

48. (New) A computer system as in claim 47, wherein said first AGP bus is a 32-bit bus or a 64-bit bus.

49. (New) A computer system as in claim 47, wherein said bridging means includes a PCI interface.

50. (New) A computer system as in claim 47, wherein said first AGP bus is the 64-bit bus performing as a first 32-bit AGP bus and a second 32-bit AGP bus, said first and said second 32-bit AGP buses capable of operating concurrently.

51. (New) A computer system as in claim 47, wherein said first AGP bus is a 64-bit bus and said bridging means comprises an ASIC that interfaces directly with said core logic, said first AGP bus performs as a superset of a standard 32-bit AGP bus.

52. (New) A computer system as in claim 47, said computer system further comprising one of a geometry processor and a rendering processor connected to said bridging means.

53. (New) A computer system as in claim 52, wherein said geometry processor and said rendering processor can communicate without using said core logic.

54. (New) A computer system as in claim 52, wherein said geometry process and said rendering processor reside on a printed circuit board.